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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

09/806779

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/SE99/01800	October 7, 1999	October 7, 1998

TITLE OF INVENTION
APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK

APPLICANT(S) FOR DO/EO/US
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Applicant herewith submits to the United States Designated/ Elected Office (DO/EO/US) the following items under 35 U.S.C. 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the international Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureaus.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 37(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). (unexecuted)

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☐ Other items or information:

INTERNATIONAL APPLICATION NO. PCT/SE99/01799	09/806779	INTERNATIONAL FILING DATE October 7, 1999	JC08 Rec'd PCT/PTO 30 MAR 2001

17. ☒ The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS				
(1)FOR	(2)NUMBER FILED	(3)NUMBER EXTRA	(4)RATE	(5)CALCULATIONS
TOTAL CLAIMS	12 - 20	0	X $ 18.00	$ 0.00
INDEPENDENT CLAIMS	2 - 3	0	X $ 80.00	0.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $ 270.00	$ 270.00

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)): **CHECK ONE BOX ONLY** ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) ..... $ 690		
☐ No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ..... $ 710		
☒ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1000		$ 1,000.00
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4) ..... $ 100		
☐ Filing with EPO or JPO search report ..... $ 860		
Surcharge of $130.00 for furnishing the National fee or oath or declaration later than 20 30 mos. from the earliest claimed priority date (37 CFR 1.492(e)).		
	TOTAL OF ABOVE CALCULATIONS	= 1,270.00
Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (Note 37 CFR 1.9, 1.27, 1.28).		- $ 635.00
	SUBTOTAL	= 635.00
Processing fee of $130.00 for furnishing the English Translation later than 20 30 mos. from the earliest claimed priority date (37 CFR 1.492(f)).		+
0	TOTAL FEES ENCLOSED	$ 635.00

a. ☐ A check in the amount of $__ to cover the above fees is enclosed.

b. ☒ Please charge Deposit Account No. 16-1150 in the amount of $ 635.00 to cover the above fees. A copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 16-1150. A copy of this sheet is enclosed.

18. ☐ Other instructions

n/a

19. ☒ All correspondence for this application should be mailed to

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NEW YORK, NEW YORK 10036-2711

20. ☒ All telephone inquiries should be made to (212) 790-2803

Garland T. Stephens		37,242	3/30/01
NAME	SIGNATURE	REGISTRATION NUMBER	DATE

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APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK

Technical Field of Invention

The present invention refers to the field of circuit switched communication networks, and, more specifically, to the field of routing data packets in a DTM network.

Background of the Invention

Today, new types of circuit-switched communication networks are being developed for the transfer of information using synchronous time division multiplexed bit-streams. Within this field, a new technology, referred to as DTM (Dynamic synchronous Transfer Mode), is currently being developed, primarily addressing the problem of providing quality of service to users of real-time, broadband applications.

The structure of a DTM network has been described in, e.g., "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and in "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2):119-139, April 1992.

The basic topology of a DTM network is preferably a bus with two unidirectional, multi-access optical fibers connecting a number of nodes. However, the topology may just as well be any other kind of structures, e.g. a ring structure or a hub structure.

The bandwidth of each wavelength on the bus, i.e. each bitstream on each fiber, is divided into recurrent essentially fixed size frames, which in turn are divided into fixed size time slots. The number of slots in a frame thus depends on the network's bit-rate. The time slots are divided into two groups, control slots and data slots. Control slots are typically used for transferring of signaling messages between said nodes for the network's internal operation. The data slots are used for

the transfer of payload data between users connected to the different nodes.

Each node is arranged to dynamically establish, terminate, and modify DTM channels by dynamically allocating time slots thereto.

When a DTM channel is used for transferring asynchronous traffic, such as TCP/IP packets, a mechanism for providing routing of said packets through the DTM network is often needed. In prior art, such a mechanism is typically provided by the addition of a dedicated router station, either directly connected to the DTM network or indirectly connected to the DTM network via, e.g. an Ethernet link connecting the router station to a DTM access device.

In this context, the use of a dedicated router station of course implies additional costs and increased network complexity. An object of the invention is therefore to provide a routing solution in a DTM network that reduces the cost for incorporation of dedicated router stations.

Summary of the invention

The above mentioned and other objects are achieved by the invention as defined in the accompanying claims.

According to a first aspect of the invention, there is provided a circuit board to be connected to a switch core and being provided with an interface for receiving one or more input DTM channels from said switch core and for transmitting one or more output DTM channels to said switch core. Furthermore, said circuit board comprises means for deriving at least a portion of a data packet received, divided into DTM time slots, in one of said input DTM channels. Also, said circuit board is provided with routing means for selecting, based upon information provided in said at least a portion of a data packet, if said data packet is to be transmitted in one or more of said output DTM channels and, if so, which one or more of

said output DTM channels said data packet is to be transmitted in, and with output means for providing one or more output DTM channels with said data packet, divided into DTM time slots, in accordance with the selection of output DTM channels made by said routing means.

The invention is thus based upon the idea of providing, in a DTM network, a routing mechanism in a circuit board designed to be received as a disconnectable module in a switch apparatus and to communicate via the switch core thereof. Thus, a network operator may add a routing mechanism to a DTM network by merely incorporating an electronic circuit board according to the invention in a typically already existing switch of the network.

Consequently, according to a second aspect of the invention, there is provided an apparatus for switching data in a communication network, said apparatus comprising: a switch core; one or more circuit boards, each providing access to one or more network links; one or more electronic circuit boards of the above mentioned kind; and means for receiving said circuit boards and for providing connectivity between said circuit boards and said switch core.

Furthermore, additional advantageous aspects has been found when designing the interface between the switch core and the electronic circuit board in such a way that complete DTM frames are exchanged.

Thus, according to a preferred embodiment according to said first aspect of the invention, said the interface of the circuit board comprises: means for receiving sequential input DTM frames from said switch core and for transmitting sequential output DTM frames to said switch core; and means for determining the existence of one or more input DTM channels transferred in said input DTM frames, and of one or more output DTM channels transferred in said output DTM frames, and said output means comprise frame generating means for generating said sequential output DTM frames and for providing DTM time

slots thereof, defining an output DTM channel, with said data packet, divided into DTM time slots, in accordance with the selection of output DTM channels made by said routing means.

Similarly, said switch core is preferably arranged to provide time and space switching between DTM ports and wherein said one or more circuit boards, which provide access to said network links, each comprises an interface for receiving sequential input DTM frames from said switch core and for transmitting sequential output DTM frames to said switch core.

One advantage of using such an interface between the circuit board and the switch core is that the protocols used to handle DTM frames at said interface may, if so desired, be designed very similar to the protocols used at any other DTM interface.

For definition, as referred to herein, a "DTM network" is a circuit switched time division multiplexed network of the kind wherein information is transferred between nodes of the network on bitstreams. Each bitstream is divided into regularly recurrent, essentially fixed size frames, so called "DTM frames", each comprising a number of fixed size time slots, said time slots being separated into control slots and data slots. Control slots are used for control signaling between nodes of the network, and data slots are used for the transfer of user data (sometimes often referred to as payload data).

Furthermore, in a DTM network, write access to the time slots of a DTM frame is distributed among nodes being attached to the bitstream carrying said DTM frame, each node typically having write access to a respective at least one control slot and a respective dynamically adjustable set of data slots within each recurrent frame. Moreover, having write access to a time slot position in a frame means having write access to said time slot position within each recurrent frame.

In a DTM network, a node will use the data slots it has write access to for establishing so called "DTM channels" by allocating one or more of said data slots to each respective DTM channel. Hence, as referred to herein, a DTM channel is defined by one or more time slots occupying the same time slot position within each DTM frame of the bitstream upon which said DTM channel is carried. However, if a DTM channel reaches, for example, over two bitstreams, the channel may of course be defined by a different set of time slot positions on the two bitstreams. Also, a DTM channel may be either a control channel or a data channel, depending on whether control or data slots that is allocated to said channel. Furthermore, a DTM channel may be uni-, multi- or broadcast.

As the demand for network capacity changes, DTM channels may be dynamically established, terminated, or modified, the latter by changing the number of time slots allocated to a DTM channel. Also, the distribution of write access to time slot among different nodes may be dynamically modified as different nodes develop different needs for control signaling and data transfer.

Consequently, a circuit board according to the invention is typically provided with means for determining which input and output channels that are to be handled by said routing processor and which that are to be bypassed, i.e. not routed via the routing processor.

The above-mentioned and other aspects and features of the invention, such as the use of a switch core memory shared by all switch ports and the use of a router memory shared by all channels accessed by the router means, will be more fully understood from the following description of embodiments thereof.

Brief Description of the Drawings

Exemplifying embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows en example of the structure of a DTM frame of a bitstream in a DTM network;

Fig. 2 schematically shows transfer of asynchronous traffic in one of the DTM channels shown in Fig. 1;

Fig. 3 schematically shows a switch equipped with a circuit board according to the invention;

Fig. 4 schematically shows an exemplifying embodiment of a circuit board according to the invention;

Fig. 5 schematically shows a switch core connected to a circuit board according to an embodiment of the invention; and

Fig. 6 schematically shows another switch core connected to a circuit board according to another embodiment of the invention.

Detailed Description of an Exemplifying Embodiment

An example of the structure of a DTM frame of a bitstream in a DTM network will now be described with reference to Fig. 1.

As shown in Fig. 1, in a DTM network, a bitstream B, interconnecting at least two bitstream access units, is divided into recurrent, essentially fixed sized DTM frames, wherein the start of each DTM frame is defined by a frame synchronization time slot F. Each DTM frame will typically have a nominal duration of 125 μs.

Each DTM frame is further divided into a plurality of fixed sized, typically 64 bit, time slots. When using said frame length of 125 μs, a time slot size of 64 bits, and a bit rate of 2 Gbps, the total number of time slots within each frame will be approximately 3900.

The time slots are divided into control slots C1, C2, C3, and C4, and data slots D1, D2, D3, and D4. The control slots are used for control signaling between the nodes of the network, whereas the data slots are used for the transfer of payload data. Each node connected to the bitstream B is typically allocated at least one control slot, i.e. each node will have write access to at least

one control slot. Furthermore, write access to data slots are distributed among the nodes connected to the bit-stream. As an example, a first node (connected to the bitstream B) will have access to a control slot C1 and a set of data slots D1 within each DTM frame of the bit-stream, another node (also connected to the bitstream) will have access to a control slot C2 and a set of data slots D2 within each DTM frame of the bitstream, and so on. The set of slots allocated to a node as control slot(s) and/or data slot(s) occupy the same respective slot positions within each DTM frame of the bitstream. Hence, in the example, said first node's control slot C1 will occupy the second time slot within each DTM frame of the bitstream.

During network operation, each node may increase or decrease its access to control slots and/or data slots, thereby re-distributing the access to control slots and/or data slots among the nodes. For example, a node having a low transfer capacity demand may give away its access to data slots to a node having a higher transfer capacity demand. Furthermore, the slots allocated to a node need not be consecutive slots, but may reside anywhere within the DTM frame.

Also, note that each DTM frame typically begins with said frame synchronization time slot, defining the frame rate on the bitstream, and ends with one or more guard band time slots G.

In Fig. 1 at (c), it is furthermore assumed that said second node, having access to its control slot C2 and its range of data slots D2, has established four channels CH1, CH2, CH3, and CH4 on the bitstream. As shown, each channel is allocated a respective set of slots. In the example, the transfer capacity of channel CH1 is larger than the transfer capacity of channel 2, since the number of time slots allocated to channel CH1 is larger than the number of time slots allocated to channel CH2. The time slots allocated to a channel occupy

the same time slot positions within each recurrent DTM frame of the bitstream.

An example of the transfer of asynchronous traffic in one of the isochronous channels carried by the bitstream B shown in Fig. 1 will now be described with reference to Fig. 2. In Fig. 2, it is assumed that the channel CH3 shown in Fig. 1 is established to carry asynchronous traffic in the form of sequentially transmitted variable size data packets, which for example could be TCP/IP packets or Ethernet frames.

Fig. 2 shows three data packets transmitted in channel CH3. Each data packet is encapsulated according to a predefined encapsulation protocol. In Fig. 2, it is assumed that the encapsulation protocol defines that each data packet shall be divided into 64 bit data blocks (corresponding to the size of a time slot), that a start_of_packet slot S is to be added to the start of each data packet, and that an end_of_packet slot E is to be added to the end of each data packet, thereby forming encapsulated data packets P1, P2, and P3. In case of gaps between packets, the bitstream is provided with so called idle slots, identifying said gaps as not providing valid data. Note that Fig. 2 only shows the sequence of sequential time slots transmitted within the channel CH3. Since Fig. 1 schematically indicates that channel CH3 comprises seven time slots within each DTM frame on bitstream B, the first seven time slots transmitted in the channel CH3, i.e. the first seven time slots in Fig. 2, will be transmitted in one DTM frame, the next seven time slots will be transmitted in the next DTM frame, and so on.

A switch equipped with a circuit board according to the invention will now be described with reference to Fig. 3. In Fig. 3, a switch apparatus 50 is shown comprising a switch casing 52, a switch power and control unit 54, an electronic circuit board 56 providing a routing mechanism according to the invention, and a DTM network interface card 58 providing access to a DTM network link.

As schematically illustrated in Fig. 3, the circuit board 56 and the DTM network interface card 58 is releasably connected to a switch core (not shown) arranged inside the switch casing 52.

An embodiment of a circuit board 110 according to an embodiment of the invention will now be described with reference to Fig. 4. In Fig. 4, the electronic circuit board 110 comprises a port 111, which in turn comprises an incoming channel interface 113 and an outgoing channel interface 114 receiving and transmitting, respectively, time slot data in DTM channels from/to a switch core (not shown). The incoming and outgoing channel interfaces will provide for synchronization of the operation of the circuit board 110 in relation to the DTM frame frequency accordance with the switch core.

The incoming channel interface and the outgoing channel interface are connected to an incoming channel manager 115 and an outgoing channel manager 116, respectively. The incoming channel manager 115 and the outgoing channel manager 116 are both connected to a routing processor 117, a shared memory 119, and a buffer manager 120. The routing processor 117 is connected to a routing memory 118. Furthermore, a controller 121 is connected to the incoming channel manager 115 as well as the outgoing channel manager 116.

In operation, the incoming channel interface 113 will receive (arrow 1) data packets, for example TCP/IP packets, from the channels monitored by said interface. Each data packet is typically encapsulated according to a predefined protocol, as described with reference to Fig. 2, and will typically be received as a set of consecutive sequential 64 bit data blocks.

The incoming channel interface 113 will then forward, with preserved sequential order, each received data block to the incoming channel manager 115 (arrow 2). Each data block forwarded to the incoming channel manager 115

is accompanied by a channel identifier, designating the channel from which it was received.

Having received sufficiently many data blocks at the head end of a data packet to be able to derive information designating the size of the data packet, the incoming channel manager will send a request (arrow 3), containing the size of the data packet, to the buffer manager 120. The request will thereby inform the buffer manager 120 that the incoming channel manager 115 needs to store a data packet of the designated size in the shared memory 119.

The buffer manager 120 will then allocate an address space of the shared memory 119 to said data packet, the size of the allocated address space not being smaller than the size of said data packet. The buffer manager 120 will then answer the request by returning (arrow 4) a start address corresponding to the start of said address space to the incoming channel manager 115.

Having received said start address from the buffer manager 120, the incoming channel manager will start writing the data blocks forming the associated data packet into the shared memory 119 (arrow 5), starting at the start address received from the buffer manager data and incrementing the address one step for each data block written into the shared memory 119.

At the same time, the incoming channel manager 115 will send the start address received from the buffer manager 120, along with the address designated in the header of the data packet, to the routing processor 117 (arrow 6).

Using the routing memory 118 (arrow 7), the routing processor 117 will, based upon the address received from the incoming channel interface 115, determine whether or not the associated data packet is to be transmitted from the outgoing channel interface 114 and, if so, which outgoing channel that is to be used when transmitting said data packet.

Having determined an outgoing channel for the data packet, the routing processor 117 will transmit a signal to the outgoing channel manager 116 (arrow 8), containing a channel identifier and the start address received from the incoming channel manager. The channel identifier identifies the outgoing channel to be used when transmitting the associated data packet address, and the start address designates where to read the associated data packet from in the shared memory 120.

Having received the outgoing channel identifier and the start address from the routing processor 117, the outgoing channel manager 116 will access the shared memory (arrow 9) and start reading (arrow 10) data blocks forming the associated data packet from the shared memory 119, beginning at the start address received from the routing processor 117 and incrementing the address one step for each data block read from the shared memory 119.

At the same time, the outgoing channel manager 116 will continuously receive requests (arrow 11) for data blocks for respective outgoing channels from the outgoing channel interface 114, said request being sent from the outgoing channel interface at the rate as DTM frames is requested for transmission to the switch core connected to the outgoing channel interface 114.

As triggered by said requests for data blocks, when said requests relates to a channel identified by the a channel identifier received form the routing processor 117, the outgoing channel manager 116 will forward (arrow 12), with preserved sequential order, each data block of the associated data packet, as read from the shared memory 119 starting at the designated start address, to the outgoing channel interface 114. The outgoing channel interface 114 will then, in turn, forward (arrow 13) the received data blocks to the respective channels on the outgoing bitstream.

Having read the last data block of a data packet from the shared memory 119, the outgoing channel manager

120 will return (arrow 14) the associated start address, which was received from the routing processor 117, to the buffer manager 120. This will inform the buffer manager that the processing of the data packet stored at the address space associated with said start address is complete and that the buffer manager is now free to allocate said address space to a new data packet received via the incoming channel interface.

Also, as is understood, the purpose of the controller 121 is, among others, to determine, based upon information provided in control signaling received in a channel from the incoming channel manager, which channels that are to be handled by the incoming channel manager 115 and the outgoing channel manager 116, i.e. which channels that are to be directed to/from the routing processor 117. If there exists a channel that is received by the incoming channel manager but is not to be provided to the routing processor, said channel is bypassed at the input/output interface 113, 114.

A switch core 203 connected to an circuit board 110 according to an embodiment of the invention will now be described with reference to Fig. 5. In Fig. 5, the switch core 203 receives time slot in DTM frames from two input ports 201a and 202a and transmits received time slot data to two output ports 201b and 202b.

Each input port 201a, 202a is arranged to write each received DTM frame into a respective frame buffer of a shared frame memory 204. The data blocks from the time slots of a DTM frame are written sequentially into corresponding time slot data fields of the respective frame buffer, i.e. one data field for each input time slot.

At the same time, two time slot selection units (not shown) are arranged to select time slot data blocks to be transmitted in output DTM frames by deciding, for each output time slot to be transmitted into the respective output DTM frame, which frame buffer, and from which time slot data entry thereof (i.e. among the presently stored

time slot data blocks from both currently stored DTM frames), time slot data slot is to be collected, or passed on, to the respective output DTM frame. Hence, each selection unit is connected to the frame memory for the selection and collection of data blocks therefrom.

In order to know which frame buffer and entry or field thereof to be used for a specific output time slot, each selection unit has access to a respective slot mapping table (not shown) that, for each time slot of the respective output DTM frame and at a respective entry, provides one field designating the entry or field of said memory to be used for collecting the given output time slot. Consequently, the selection unit will pick data blocks in given output order for each time slot of the output DTM frame to receive time slot data blocks. Of course, the switch will only transmit data blocks into those slots of the output DTM frame that are allocated for that purpose.

Furthermore, as schematically illustrated in Fig. 5, a circuit board 110 according to the invention, and thus being equipped with routing means, for example as described with reference to Fig. 4, is connected to the input/-output ports 201, 202 of the switch and is arranged to received DTM frames from, and transmit DTM frames to, the switch core 203. Also, the above mentioned selection unit will determine which time slots that go into the DTM frames delivered to the circuit board 110.

In the situation shown in Fig. 5, a channel defined by time slot 7 of DTM frames received on port 201a is read to the output port 202b, more specifically to the second time slot of the DTM frame delivered therefrom, and is received by the routing circuit board 110. Based upon routing decisions, the routing circuit board 110 will transmit data packets received on said time slot 2 of the DTM frame at port 202b to either a channel defined by time slot 2 or a channel defined by time slot 3 of the DTM frame on port 202a, said channels then being mapped

into time slot 6 and 7, respectively, of the output DTM frame on port 201b. Consequently, a data packet received on the channel defined by time slot seven on port 201a will be routed to the channel defined by time slot 6 or the channel defined by time slot 7 on the output port 201b. (As is understood in Fig. 5, the routing circuit board will receive and transmit entire DTM frames from/to the switch core. However, it will typically only read data from and transmit data into time slot thereof that define channels that the routing circuit board 100 is currently configured to provide routing in relation to.)

Also, in the situation shown in Fig. 5, the selection unit is set so that time slot seven of the DTM frame received on port 201b is also, in addition to what has been described above, mapped to time slot five on the DTM frame on port 201b. Thus, packets received on the channel defined by time slot seven at port 201a is always transmitted on the channel defined by time slot five at port 201b in a circuit switched manner, irrespective of the routing decisions made by the routing circuit board 110.

As is understood, even though the channels described with reference to Fig. 5 is defined by one single time slot, they could just as well comprise any number of time slots within each frame, as dynamically selected in a DTM network.

Fig. 6 shows another embodiment solution wherein the switch core 203 of a switch is realized in form of a DTM ring/bitstream 205 connecting all ports, said ports acting as nodes on said internal DTM ring. As schematically illustrated, each time slot of the input ports 201a and 201b is written into a respective time slot of the internal DTM bitstream frame. Each output port 201b, 202b then reads selected time slots of the internal DTM bitstream 205 when transmitting output DTM frames. Moreover, the routing circuit board connected to the switch core is arranged to receive data packets from channels defined by time slots on the internal DTM bitstream 205 and to route

said data packets to channels similarly defined by time slots on the internal DTM bitstream.

As an example, in the situation illustrated in Fig. 6, an input channel defined by time slots five and six at port 202a is mapped into time slots 12 and 13 of the internal DTM bitstream 205 and is read by the routing circuit board 110. The circuit board 110 then routes said data packets to, for example, a channel defined by time slot 17 of the internal bitstream, said channel then being mapped into an output channel defined by time slot five as well as an output channel defined by time slot six of the output DTM frame at port 202b.

Even though the invention has been described above with reference to exemplifying embodiments thereof, these are not to be considered as limiting the scope of the invention. Consequently, as understood by those skilled in the art, different modifications, combinations and alterations may be made within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. A circuit board (56; 110) to be connected to a switch core, said circuit board comprising:

an interface (111) for receiving one or more input DTM channels from said switch core and for transmitting one or more output DTM channels to said switch core;

means (115) for deriving at least a portion of a data packet received, divided into DTM time slots, in one of said input DTM channels;

routing means (117) for selecting, based upon information provided in said at least a portion of a data packet, if said data packet is to be transmitted in one or more of said output DTM channels and, if so, which one or more of said output DTM channels said data packet is to be transmitted in; and

output means (116) for providing one or more output DTM channels with said data packet, divided into DTM time slots, in accordance with the selection of output DTM channels made by said routing means.

2. A circuit board as claimed in claim 1, wherein said interface comprises:

means (113, 114) for receiving sequential input DTM frames from said switch core and for transmitting sequential output DTM frames to said switch core; and

means (121) for determining the existence of one or more input DTM channels transferred in said input DTM frames, and of one or more output DTM channels transferred in said output DTM frames,

and wherein said output means comprise:

frame generating means (114) for generating said sequential output DTM frames and for providing DTM time slots thereof, defining an output DTM channel, with said data packet, divided into DTM time slots, in accordance with the selection of output DTM channels made by said routing means.

3. A circuit board as claimed in claim 1 or 2, comprising a memory (119) for temporarily storing data packets at respective memory locations thereof, wherein said interface comprises means (115) for writing said data packet into an allocated memory location of said memory when receiving said data packet and wherein said frame generating means comprises means for reading said data packet from said allocated memory location for transmission in accordance with the selection of output DTM channels made by said routing means.

4. A circuit board as claimed in claim 3, further comprising a storage manager (120) arranged to temporarily allocate a memory location of said memory for storing said data packet and to provide said interface with information designating said memory location.

5. A circuit board as claimed in claim 4, wherein said memory location is allocated by said storage manager for storing said data packet as a result of a request made by said interface when receiving said data packet.

6. A circuit board as claimed in any one of the preceding claims, comprising means (121) for determining which input and output channels that are to be handled by said routing processor and which that are to be bypassed.

7. A circuit board as claimed in any one of the preceding claims, wherein said data packet, when transmitted within said channel, is encapsulated according to a DTM encapsulation protocol.

8. An apparatus (50) for switching data in a communication network, comprising: a switch core (203); one or more circuit boards (58), each providing access to one or more network links; one or more circuit boards (56; 110)

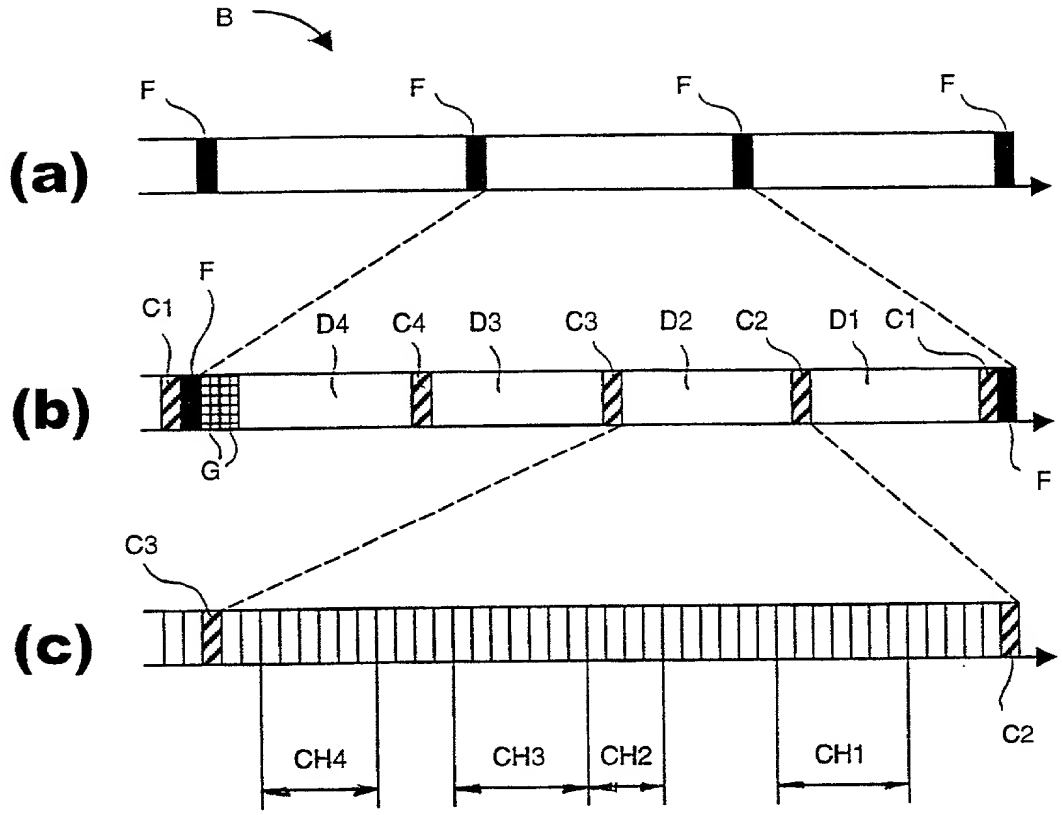
as claimed in any one of the preceding claims; and means for receiving said circuit boards and providing connectivity between said circuit boards and said switch core.

9. An apparatus as claimed in claim 8, wherein said switch core is arranged to provide time and space switching with respect to DTM frames and wherein said one or more circuit boards, which provide access to said network links, each comprises an interface for receiving sequential DTM frames from said switch core and for transmitting sequential DTM frames to said switch core.

10. An apparatus as claimed in claim 9, wherein said switch core comprises a memory (204) having a number of memory locations, each being associated with a respective circuit board, and wherein said means for providing connectivity between said circuit boards and said switch core comprise DTM frame receiving and generating means, each associated with a respective circuit board and each having write access to a respective one of said memory locations, for writing DTM frames received from the respective circuit board thereinto, and having read access to all of said memory locations, for reading time slot data from selected DTM time slot fields thereof when generating DTM frames to be delivered to the respective circuit board.

11. An apparatus as claimed in claim 10, comprising means for establishing DTM channels between circuit boards by determining which memory fields of said memory that said DTM frame receiving and generating means are to read data from when generating DTM frames to be delivered to respective circuit boards.

12. An apparatus as claimed in any one of the preceding claims, wherein said switch core is circuit switched.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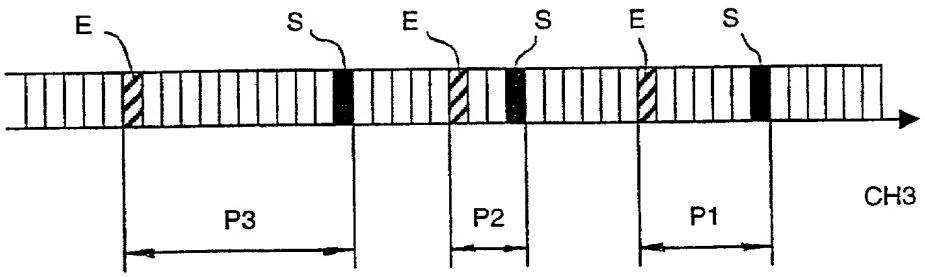
F
F
F
(a)
C1
F
D4
C4
D3
C3
D2
C2
D1
C1
(b)
G
F
C3
(c)
C2
CH4
CH3
CH2
CH1

Fig. 1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S
E
S
E
S
CH3
P3
P2
P1

Fig. 2

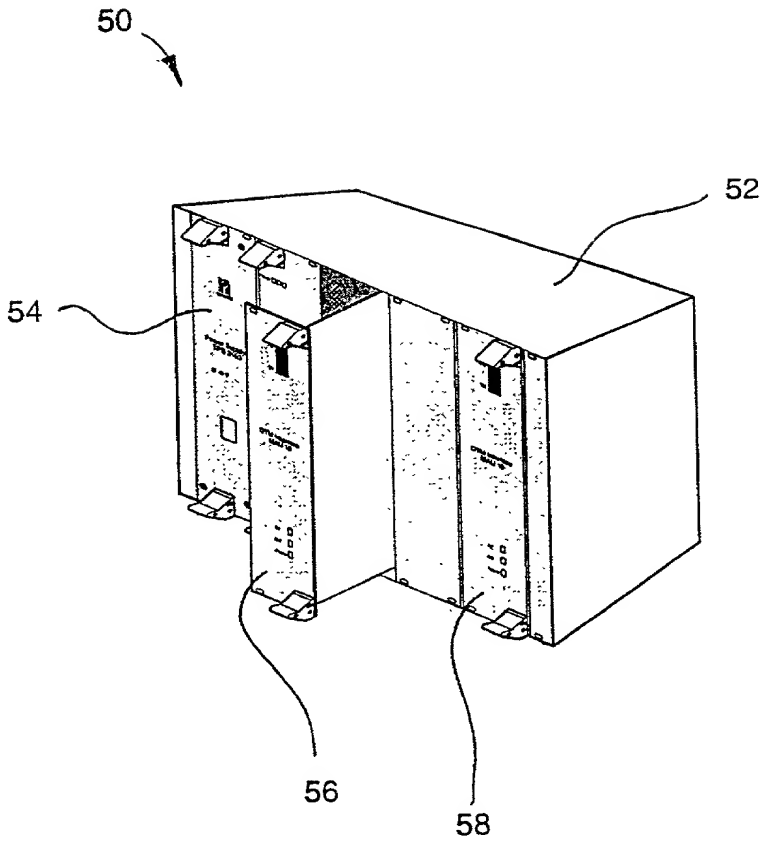
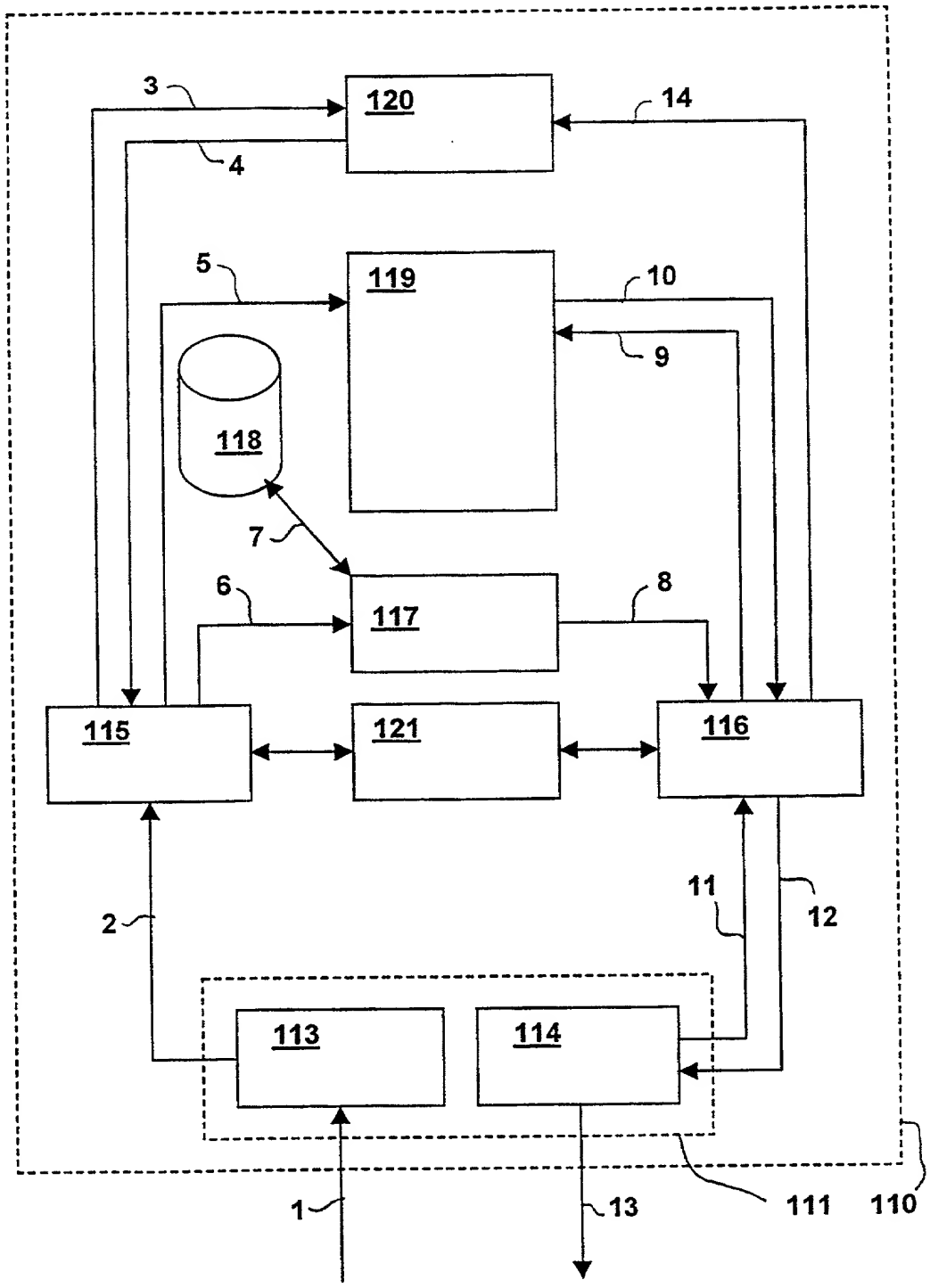


Fig. 3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14
4
5
119
10
9
118
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6
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8
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121
116
2
11
12
113
114
1
13
111
110

Fig. 4

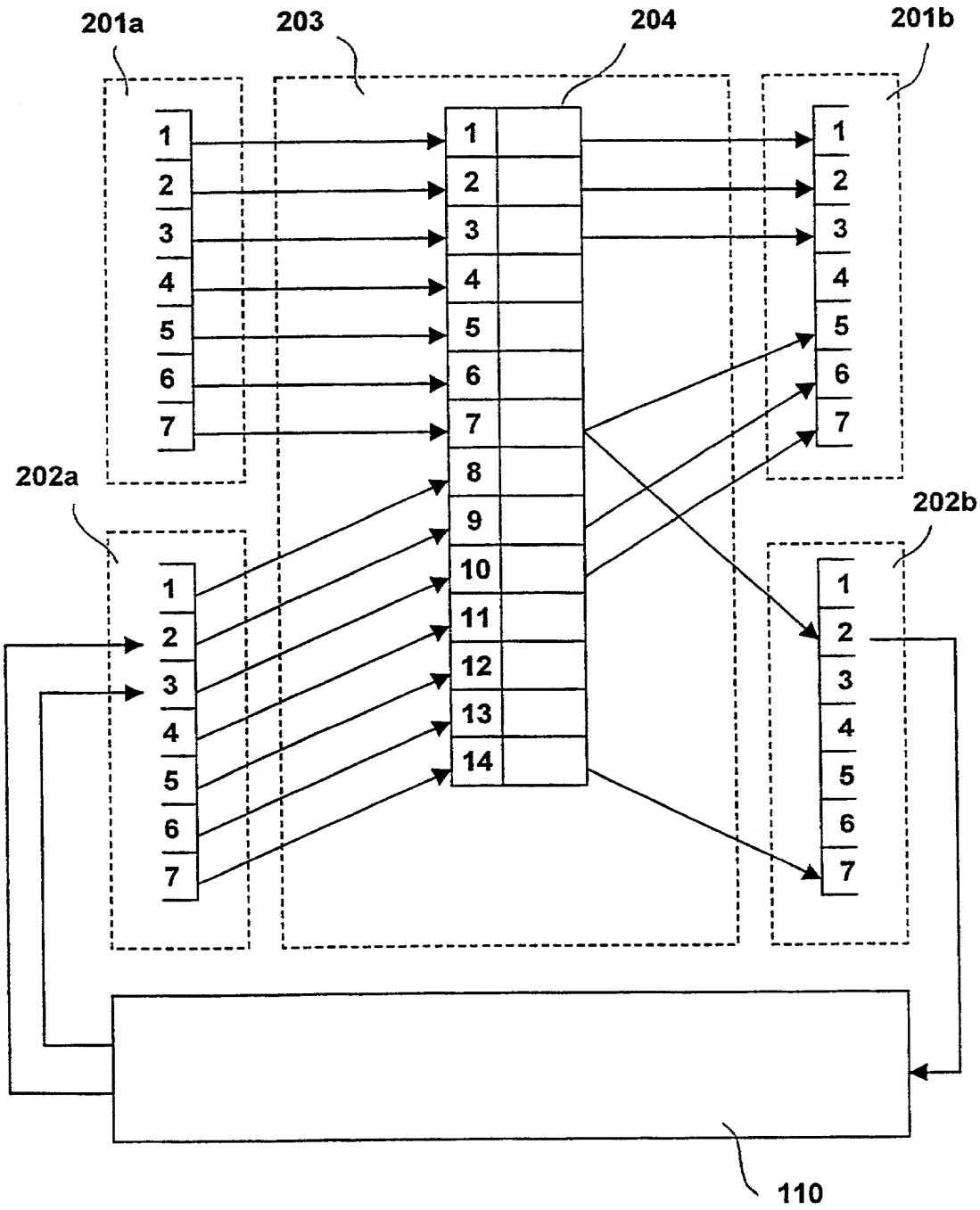

Fig. 5

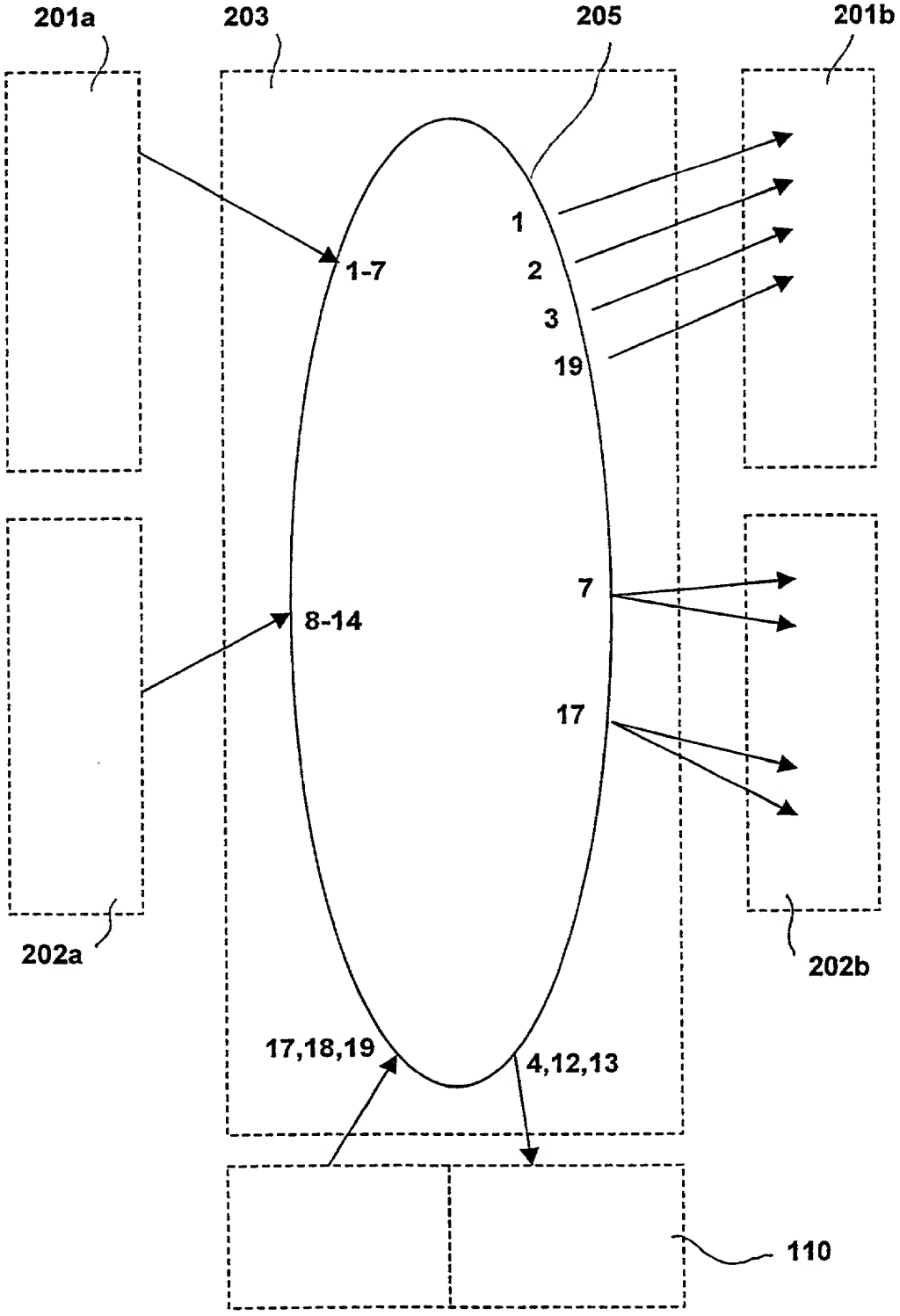

Fig. 6

DECLARATION FOR NON-PROVISIONAL PATENT APPLICATION*

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below at 201 et seq. beneath my name.

I believe I am the original, first and sole inventor if only one name is listed at 201 below, or an original, first and joint inventor if plural names are listed at 201 et seq. below, of the subject matter which is claimed and for which a patent is sought on the invention entitled

APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK

and for which a patent application:
☐ is attached hereto and includes amendment(s) filed on *(if applicable)*
☒ was filed in the United States on March 30, 2001 as Application No. TBA
☒ was filed as PCT international Application No. PCT/SE99/01800 on October 7, 1999

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
9803419-2	Sweden	October 7, 1998	YES ☒ NO ☐
PCT/SE99/01800	PCT	October 7, 1999	YES ☒ NO ☐
			YES ☐ NO ☐

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

PROVISIONAL APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NON-PROVISIONAL APPLICATION SERIAL NO.	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED

* for use only when the application is assigned to a company, partnership or other organization.

(Reg. No. 33607), Gary S. Williams (Reg. No. 31066), Ann L. Gisolfi (Reg. No. 31956), Todd A. Wagner (Reg. No. 35399), Scott B. Familant (Reg. No. 35514), Kelly D. Talcott (Reg. No. 39582), Francis D. Cerrito (Reg. No.38100), Anthony M. Insogna (Reg. No. 35203), Brian M. Rothery (Reg. No. 35340), Brian D. Siff (Reg. No. 35679), Alan Tenenbaum (Reg. No. 34939), Michael J. Lyons (Reg. No. 37,386), Garland T. Stephens (Reg. No. 37,242) and William J. Sipio (Reg. No. 34,514), all of Pennie & Edmonds LLP, whose addresses are 1155 Avenue of the Americas, New York, New York 10036, 1667 K Street N.W., Washington, DC 20006 and 3300 Hillview Avenue, Palo Alto, CA 94304, all of Pennie & Edmonds LLP (PTO Customer No. 20583), as its attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. 3.71, provided that, if any one of these attorneys ceases being affiliated with the law firm of Pennie & Edmonds LLP as partner, counsel, or employee, then the appointment of that attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated.

[ ] An assignment of the entire interest in the above-identified subject application was recorded on _____ at reel/frame _/_____.

[ ] An assignment of the entire interest in the above-identified subject application is submitted herewith for recording.

[x] A copy of an assignment of the entire interest in the above-identified subject application is submitted herewith. The assignment will be duly recorded.

Please direct all correspondence for this application to customer no. 20583.

ASSIGNEE: NET INSIGHT AB

Signature: _____

Typed Name: BENGT OCSSON

Position/Title: CEO

Address: P.O. Box 42093

SE-126 14 Stockholm, Sweden

Date: MAY 5, 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Lindgren et al.

Application No.: TBA

Group Art Unit: TBA

Filed: March 30, 2001

Examiner: TBA

For: APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK

Attorney Docket No.: 10806-005

POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR(S) UNDER 37 C.F.R. 3.71

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned assignee of the entire interest in the above-identified subject application hereby appoints: S. Leslie Misrock (Reg. No. 18872), Berj A. Terzian (Reg. No. 20060), David Weild, III (Reg. No. 21094), Jonathan A. Marshall (Reg. No. 24614), Barry D. Rein (Reg. No. 22411), Stanton T. Lawrence, III (Reg. No. 25736), Charles E. McKenney (Reg. No. 22795), Philip T. Shannon (Reg. No. 24278), Francis E. Morris (Reg. No. 24615), Charles E. Miller (Reg. No. 24576), Gidon D. Stern (Reg. No. 27469), John J. Lauter, Jr. (Reg. No. 27814), Brian M. Poissant (Reg. No. 28462), Brian D. Coggio (Reg. No. 27624), Rory J. Radding (Reg. No. 28749), Stephen J. Harbulak (Reg. No. 29166), Donald J. Goodell (Reg. No. 19766), James N. Palik (Reg. No. 25510), Thomas E. Friebel (Reg. No. 29258), Laura A. Coruzzi (Reg. No. 30742), Jennifer Gordon (Reg. No. 30753), Geraldine F. Baldwin (Reg. No. 31232), Victor N. Balancia (Reg. No. 31231), Samuel B. Abrams (Reg. No. 30605), Steven I. Wallach (Reg. No. 35402), Marcia H. Sundeen (Reg. No. 30893), Paul J. Zegger (Reg. No. 33821), Edmond R. Bannon (Reg. No. 32110), Bruce J. Barker (Reg. No. 33291), Adriane M. Antler (Reg. No. 32605), Thomas G. Rowan (Reg. No. 34419), James G. Markey (Reg. No. 31636), Thomas D. Kohler (Reg. No. 32797), Scott D. Stimpson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: ☒ Application of: Lindgren et al.
☐ Patent of:

☒ Application No.: TBA
☐ Patent No.:

Group Art Unit: TBA

☒ Filed: March 30, 2001
☐ Issued:

Examiner: TBA

For: APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK

Attorney Docket No.: 10806-005

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
[37 CFR 1.9(f) and 1.27(c)] - Small Business Concern

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I hereby declare that I am

☐ the owner of the small business concern identified below:
☐ an official of the small business concern empowered to act in behalf of the concern identified below:

Name of organization Net Insight AB
Address of organization P.O. Box 42093
SE-126 14 Stockholm
Sweden

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the person employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern and/or there is an obligation under contract or law by the inventor(s) to convey rights to the small business concern with regard to the invention entitled APPARATUS FOR ROUTING DATA PACKETS IN A DTM NETWORK by inventor(s) Lindgren et al. described in

☐ the specification filed herewith
☒ application no. TBA filed March 30, 2001
☐ patent no. issued

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below and no rights to the invention are held by any person, other than the inventor, who could not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

FULL NAME_____
ADDRESS_____

_____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME_____
ADDRESS_____

_____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME_____
ADDRESS_____

_____

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. [37 CFR 1.28 (b)]

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, and patent issuing thereon, or any patent to which this verified statement is directed.

Send correspondence to: PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, N.Y. 10036-2711

Direct Telephone calls to:
PENNIE & EDMONDS LLP
(212) 790-9090

Name of person signing BENGT OLSSON
Title of person other than owner CEO
Address of person signing P.O. Box 42093, SE-126 14 Stockholm, Sweden
Signature _____ Date MAY 5, 2001

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)